

FIG. 1A

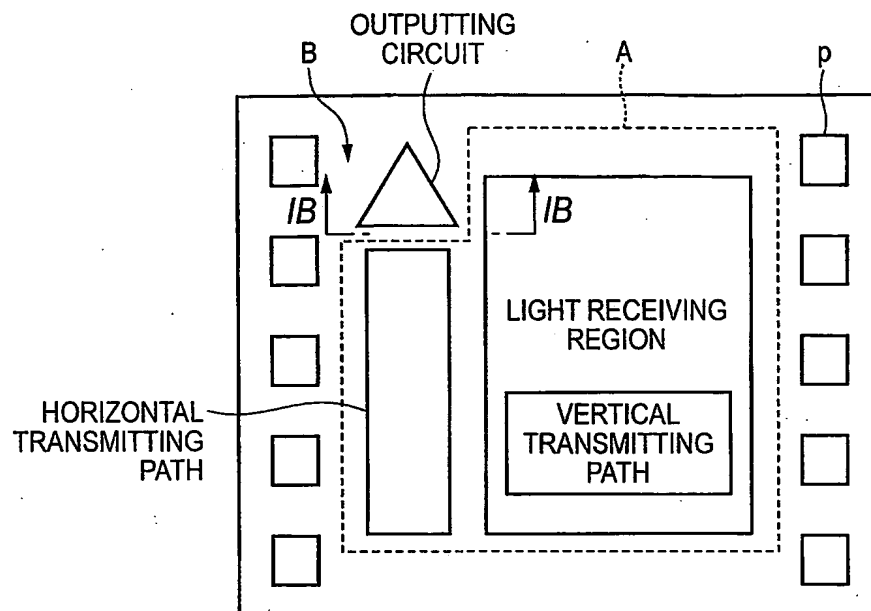


FIG. 1B

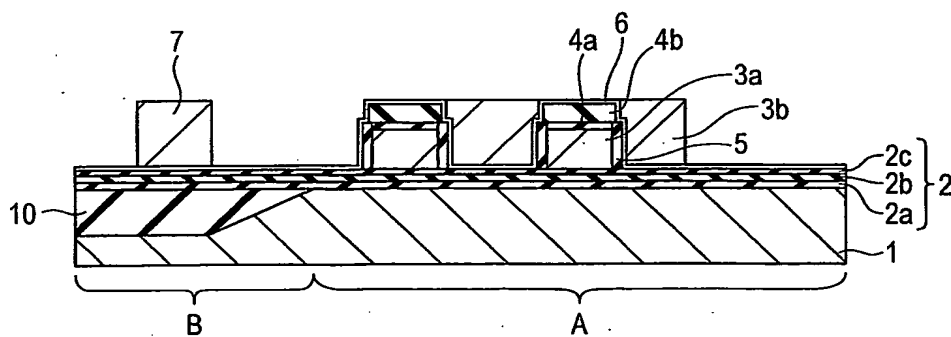


FIG. 2A

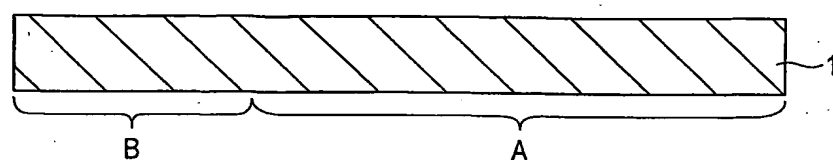


FIG. 2B

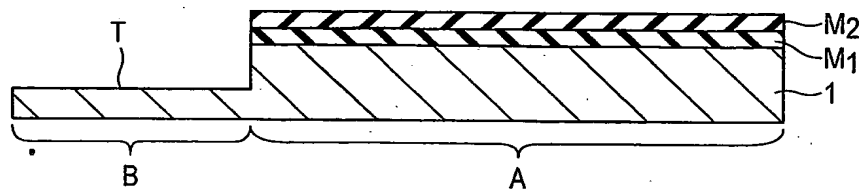


FIG. 2C

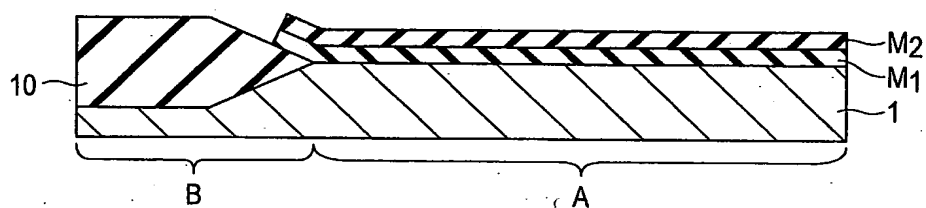


FIG. 2D

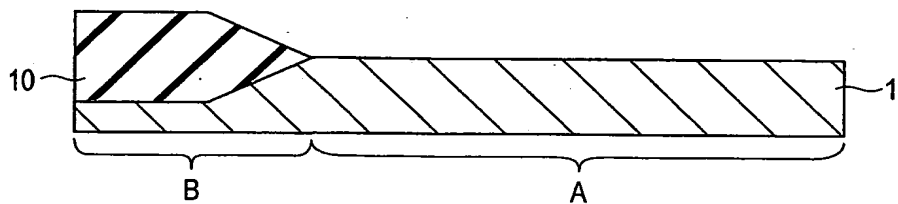


FIG. 2E

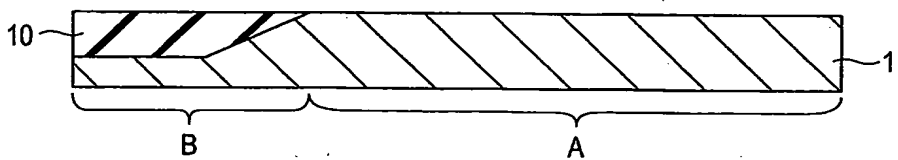


FIG. 3A

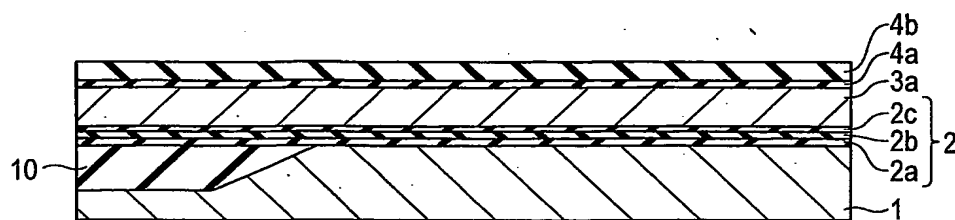


FIG. 3B

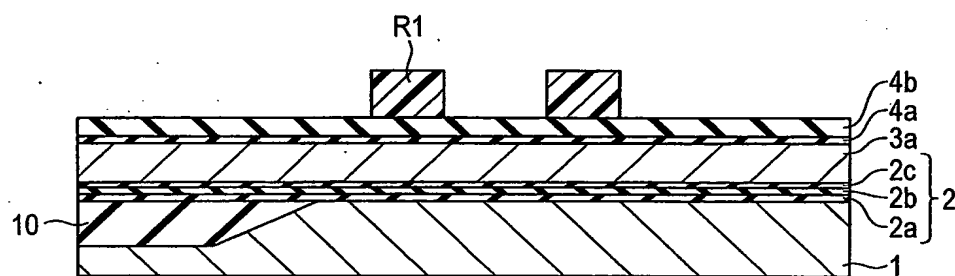


FIG. 3C

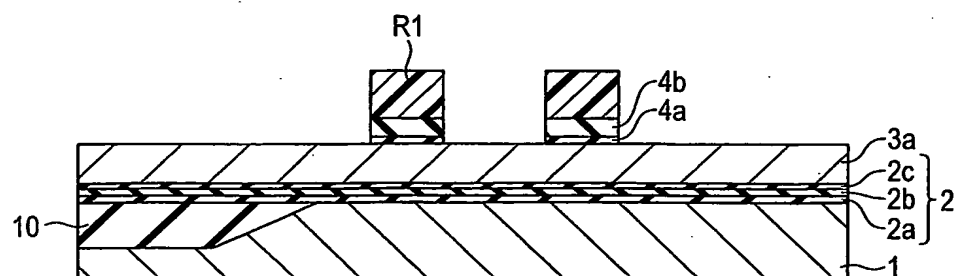


FIG. 4D

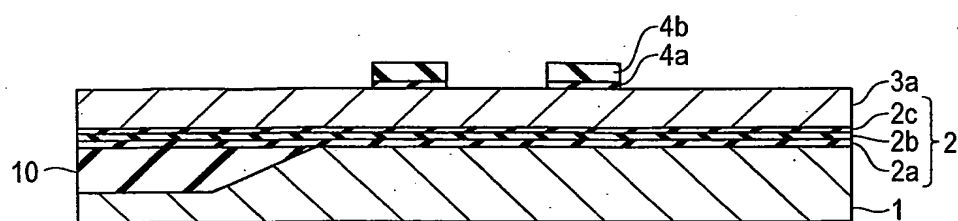


FIG. 4E

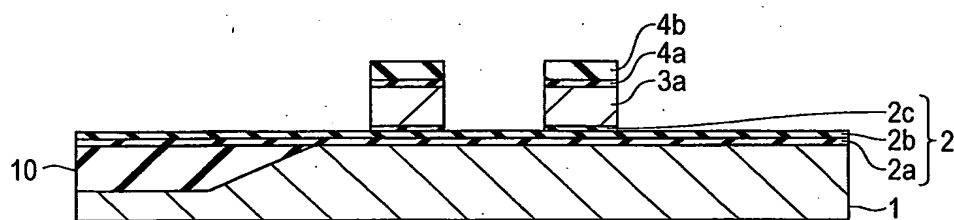


FIG. 4F

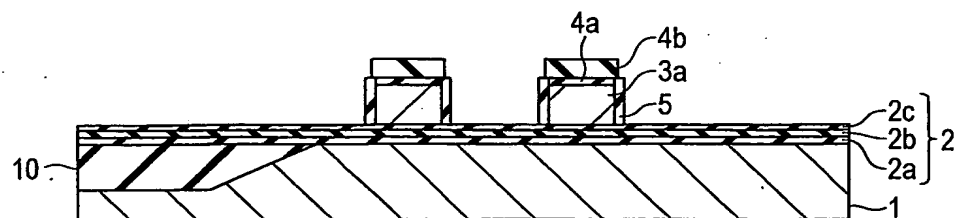


FIG. 5G

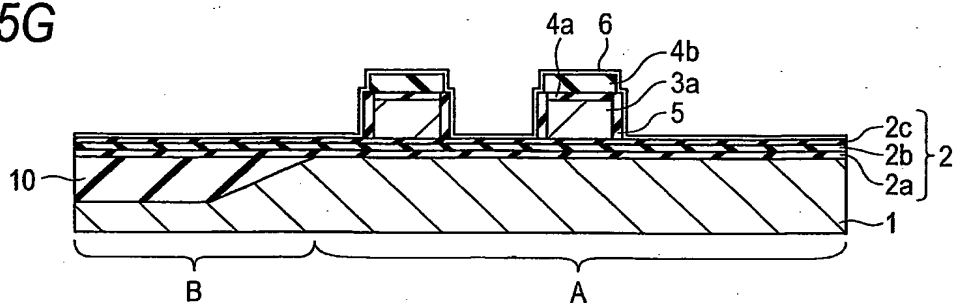


FIG. 5H

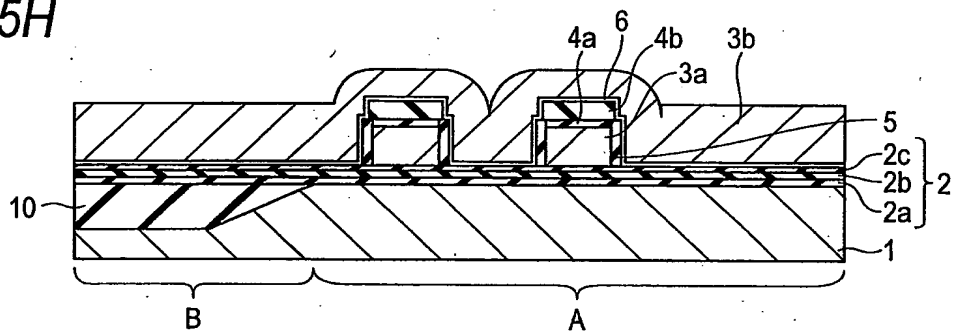


FIG. 5I

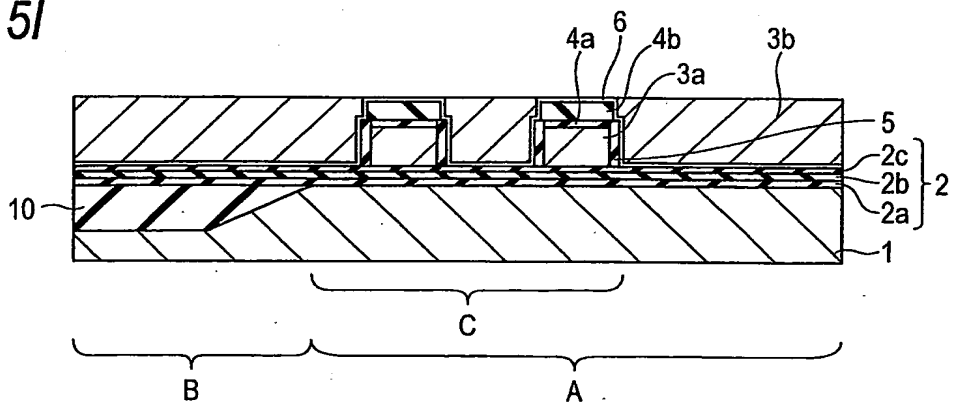
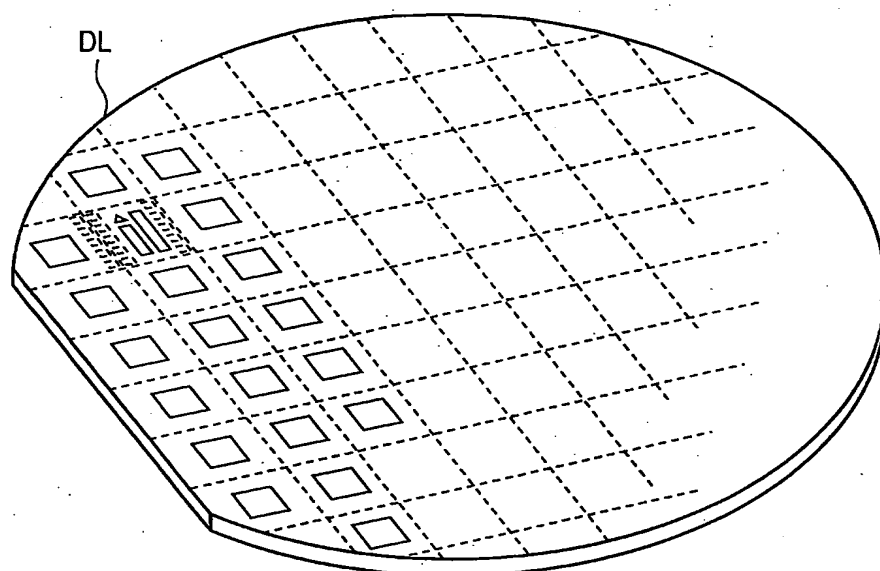




FIG. 7



A cross-sectional view of a semiconductor device. A substrate 1 is shown with a thin layer 2 on its top surface. Layer 2 is composed of sub-layers 2a, 2b, and 2c. On the left, a region labeled B contains a component 20 and a layer T. On the right, a region labeled A contains a series of components: 3a, 3b, 4a, 4b, 5, 6, and 7. The components 3a and 3b are adjacent to the thin layer 2, while 4a, 4b, 5, 6, and 7 are stacked or positioned above them.



FIG. 9

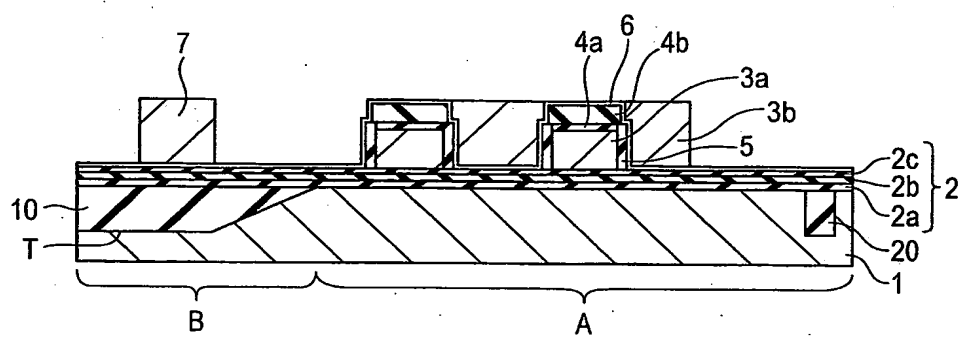


FIG. 10A

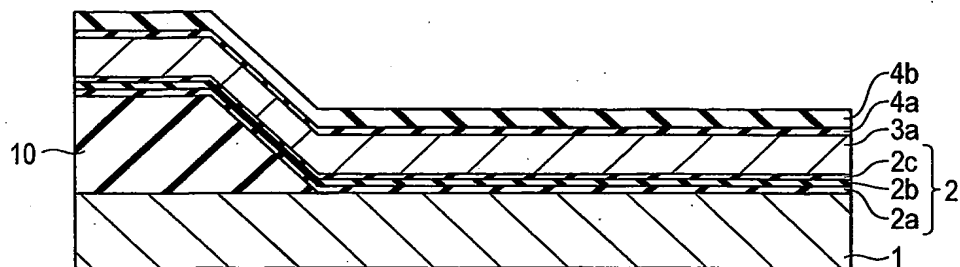


FIG. 10B

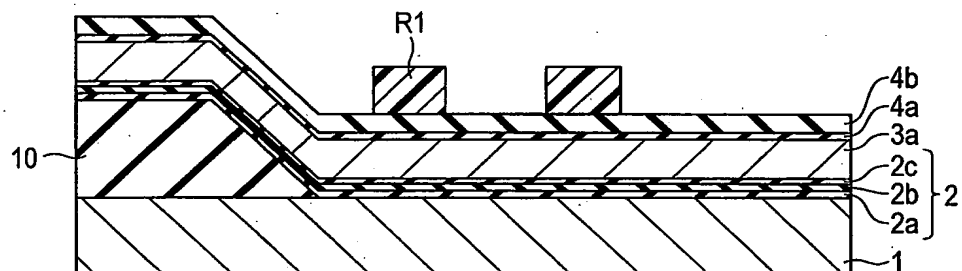


FIG. 10C

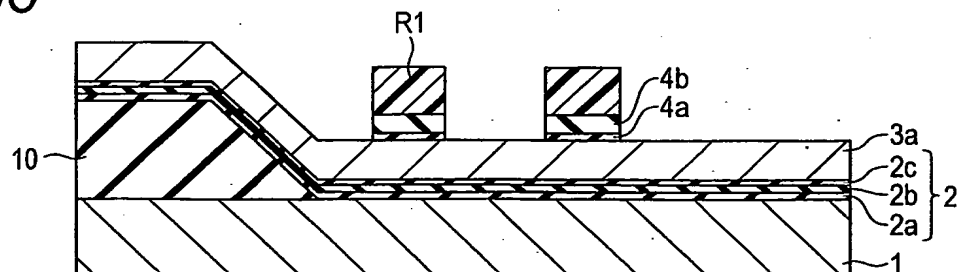


FIG. 11D

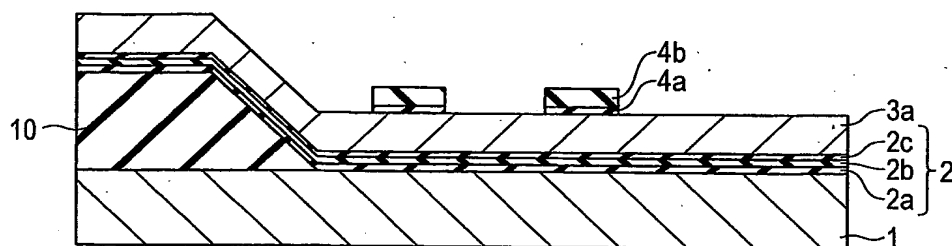


FIG. 11E

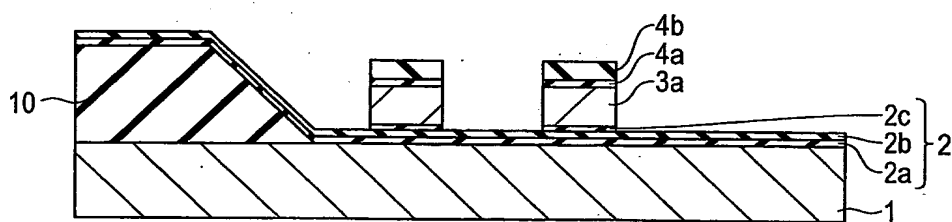


FIG. 11F

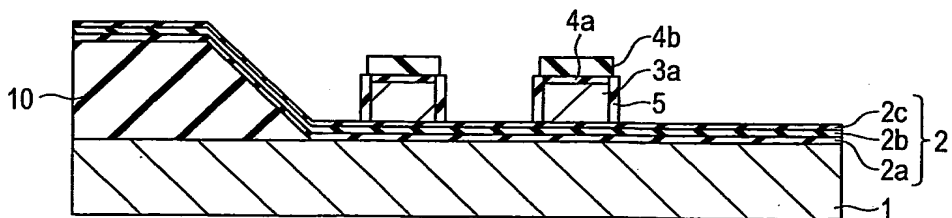


FIG. 12G

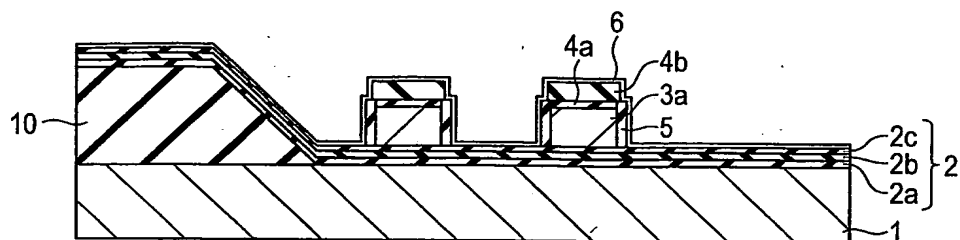


FIG. 12H

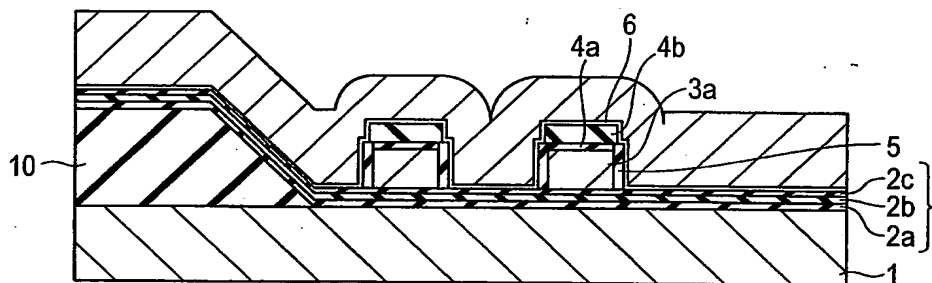


FIG. 12I

